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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/805,827	03/14/2001	Viktor M. Hungerbuehler	33307	4452

116 7590 08/27/2003

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EXAMINER

HUYNH, KIM T

ART UNIT

PAPER NUMBER

2189

DATE MAILED: 08/27/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

9/15/98

Office Action Summary

Application No.

09/805,827

Applicant(s)

HUNGERBUEHLER ET AL.

Examiner

Kim T. Huynh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 March 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2, 3.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for priority; Regulations under the PCT. See 37 CFR 1.55(a)(1)(ii)

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 20 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. "signal of the type ECL".

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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4. Claims 1, 3-15, 19, 22-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. (US Patent 6,587,909) in view of Salo et al. (US Patent 6,202,109)

As per claim 1, Olarig discloses data acquisition module for modular data acquisition system comprising:

- connecting means on a first side for removably inserting the module in a slot of said modular acquisition system, (col.1, lines 42-63)
- at least one clock generating circuit capable of supplying an internal clock signal, (col.8, line 67-col.9, line 36)
- wherein at least one connector makes it possible to plug in a removable connecting element on a second external side of said module different from the first side in order to connect said module to a synchronization bus connecting several modules in said system, said connection being effected independently from the insertion of said module into said slot, (col.3, lines 20-55), (col.6, line 27 col.7, line 16)
- and wherein a clock selecting circuit allows the selection of either a slave-clock state, in which said converters are synchronized by said synchronization bus, or of a master-clock state in which these converters are synchronized by said internal clock signal that is also used as external synchronization signal on said synchronization bus. (col.9, line 65-col.10, line 30), (col.3, lines 20-55), (col.6, line 28-col.7, line 16)

Olarig discloses all the limitations as above except analog-to-digital converter for converting an analog input signal into a digital signal.

However, Salo discloses in digital signal processing unit, there is a need for analog/digital converters (A/D) for converting analog signals into digital form, and digital/analog converters (D/A) for converting a digital signal into analog form into a signal to be transmitted. (col.8, line 64-col.9, line 35)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Olarig's teaching into Salo's method so as to give significant advantages; a codec and an audio connection can be eliminated from the expansion card which becomes simpler and less expensive and further, the application will not require considerable changes in the hardware or software of current expansion cards. (col.2, lines 23-29)

As per claim 3, Olarig discloses wherein a delay element enables the external synchronization signal received from the synchronization bus to be delayed. (col.34, line 52-col.35, line 21)

As per claim 4, Olarig discloses wherein the delay applied by said delay element can be programmed. (col.34, line 52-col.35, line 21)

As per claim 5, Olarig discloses wherein said connector comprises a trigger input for transmitting at least one trigger signal between adjacent modules. (col.3, line 20-col.4, line 45), (col.6, line 28-col.7, line 16)

As per claim 6, Olarig discloses wherein at least one trigger generating circuit enables a trigger signal to be generated in response to a predefined event on one of the acquisition channels. (col.6, line 28-col.7, line 16)

As per claim 7, Olarig discloses wherein a trigger selecting circuit makes it possible to impose on said synchronization bus the trigger signal supplied by said trigger generating circuit. (col.6, line 28-col.7, line 16)

As per claim 8, Olarig discloses wherein said external synchronization signal can momentarily be interrupted. (col.5, line 44-col.7, line 16)

As per claim 9, Olarig discloses wherein said external synchronization signal can be interrupted according to the state of said trigger signal. (col.5, line 44-col.7, line 16)

As per claim 10, Olarig discloses wherein said clock selecting circuit can be controlled by signals applied on said connecting means. (col.5, line 44-col.7, line 16)

As per claim 11, Olarig discloses wherein the delay element can be controlled by signals applied on said connecting means. (col.5, line 44-col.7, line 16), (col.34, line 52-col.35, line 21)

As per claim 12, Olarig discloses wherein said trigger selecting circuit can be controlled by signals applied on said connecting means. (col.5, line 44-col.7, line 16)

As per claim 22, Olarig discloses wherein a plurality of modules are connected two by two by connecting elements comprising each a first series of pins plugged

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in a connector on said second front side of a first acquisition module and a second series of pins plugged in a connector on said second front side of a second acquisition module. (col.3, lines 11-55)

As per claims 13, 25, Olarig discloses wherein said connector makes it possible to simultaneously plug in two removable connecting elements enabling said external synchronization signal and/or said trigger signal to be transmitted from or to two adjacent modules in said modular acquisition system. (col.3, lines 11-55)

As per claims 14, 26, Olarig discloses wherein at least one acquisition channels comprises:

- at least a memory element for storing the demultiplexed signal supplied by said demultiplexer, (col.24, lines 30-67)
- wherein said trigger generating circuit is connected at the output of the demultiplexer. (col.24, lines 30-67)

As per claim 15, Olarig discloses wherein confirms to the PCI standard, (col.14, lines 46-67)

And wherein said connector is placed on said second side on the front of said module that can be accessed by the user when said module is mounted in said modular acquisition system. (col.3, lines 46-55)

As per claim 19, Olarig discloses wherein said external synchronization signal is a differential signal. (col.5, line 38-col.7, line 16)

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As per claim 21, Olarig discloses wherein several phase-shifted external synchronization signals can be transmitted on said bus. (col.10, lines 31-62)

As per claim 23, Olarig discloses the modular system further comprising a clock module for supplying an external synchronization signal to one or several modules in a modular data acquisition system, wherein said clock module comprises:

- connecting means for removably inserting the clock module in a slot of said modular acquisition system, (col.3, lines 11-55)
- at least one clock generating circuit capable of supplying an external synchronization signal, (col.8, line 67-col.9, line 36)
- at least one connector for plugging in a removable connecting element on one of said second external sides of said clock module in order to transmit said external synchronization signal on a bus connecting adjacent modules in said modular acquisition system. (col.3, lines 20-55), (col.6, line 27 col.7, line 16)

As per claim 24, Olarig discloses the modular system further comprising a trigger module for supplying a trigger signal to one or several modules in a modular data acquisition system, wherein said trigger module comprises:

- connecting means for removably inserting the trigger module in a slot of said modular acquisition system, (col.3, line 20-col.4, line 45), (col.6, line 28-col.7, line 16)

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- a trigger generating circuit capable of generating a trigger signal in response to a predefined event on an acquisition channel of the modular acquisition system, (col.6, line 28-col.7, line 16)
- at least one connector for plugging in a removable connecting element on one of said second external sides of said trigger module in order to transmit a trigger signal on a bus connecting adjacent modules in said modular acquisition system. (col.3, lines 20-55), (col.6, line 27 col.7, line 16)

As per claim 27, Olarig discloses wherein said removable connecting element comprises:

- a printed circuit board comprising a plurality of paths enabling said pins of the first series to be electrically connected with said pins of the second series,(fig.5), (col.3, lines 20-55), (col.5, lines 38-51)
- at least a protrusion designed to be plugged in one of said acquisition modules so as to prevent said removable connecting element from turning. (col.3, lines 20-55), (col.5, lines 38-51)

As per claim 28, Olarig discloses wherein said connection element comprises a housing of plastic material encasing said printed circuit board. (col.3, lines 11-55)

As per claim 29, Olarig discloses wherein it comprises at least one connecting element provided with at least one terminating impedance electrically connected between one of said pins and an earth signal, the value of said terminating

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impedance being about equal to the line impedance of the signal traveling through the pin in question. (col.7, lines 5-67)

As per claim 30, Olarig discloses wherein the shape of said connecting element with at least one terminating impedance does not allow it to be plugged in between two other connecting elements. (col.8, lines 19-67)

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. (US Patent 6,587,909) in view of Salo et al. (US Patent 6,202,109), and further in view of Shah et al. (US Patent 6,141,711)

Olarig discloses all the limitations as above except clock generating circuit comprises a phase lock loop. However, Shah discloses bus controller allowing the internal clock and phase locked loop (PLL) within bus controller sufficient time to synchronize. (col.7, lines 6-14)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Shah's teaching into Olarig's method so as to allowing insertion and removal of a device card or the like to or from a computer system without interrupting operation of the computer system. (col.1, lines 17-24)

6. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. (US Patent 6,587,909) in view of Salo et al. (US Patent 6,202,109), and further in view of Applicant Admitted Prior Art (AAPA)

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Olarig discloses wherein said connector is placed on said second side on the front of said module that can be accessed by the user when said module is mounted in said modular acquisition system. (col.3, lines 46-55)

Olarig discloses all the limitations as above except wherein it conforms to the CompactPCI, PXI, or VXI standards. However, Applicant Admitted Prior Art notes at page 1, acquisition modules conform to the PCI, CompactPCI, VXI or PXI standards are known.

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate AAPA's teaching into Olarig's method so as to have advantage that the user can configure them by adding or replacing certain modules and that they can thus be adapted to the most diverse needs. (see page 1, related art)

Conclusion

7. A shortened statutory period for reply is set to expire *THREE* months from the mailing date of this communication. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after *SIX* (6) months from the mailing date of this communication. If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. If no period for reply is specified above, the maximum statutory period will apply and will expire *SIX* (6) months from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become *ABANDONED* (35 U.S.C 133).

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Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

8. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.*

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7249 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

August 21, 2003



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